REMARKS/ARGUMENTS

This is in response to an Office action dated 11/28/2006.

Status
Claims 1-20 are pending
Claims 1-8 (method) are withdrawn from consideration
Claims 9-20 (apparatus) are rejected

Election/Restrictions

In the Response to Restriction Requirement dated 09/8/2006, Applicant has elected without traverse the invention of Group II (Claims 9-20) drawn to a device is acknowledged. Accordingly, claims 1-8 (Group I, Method) are withdrawn from consideration as being directed to a non-elected invention. Applicant has the right to file a divisional application covering the subject matter of the non-elected claims 1-8, drawn to a method.

Claims 1-8 are canceled herewith.

Rejection(s) under 35 USC 103

Claims 9-11 and 14 are rejected under 35 U.S.C. 102(e) as being anticipated by Fujimaki '725. The Examiner states that,

> Fujimaki discloses a bipolar device comprising a collector region (fig. 2, NPN transistor, 105), a base film (fig. 4, 118b) disposed atop the collector region; an emitter structure (fig. 4, 122) formed atop the base layer; and a nitride stress film (fig. 4, 117) disposed adjacent the emitter structure and atop the base film; wherein the stress film is disposed in close proximity to an intrinsic portion of the device (p-n junctions form intrinsic regions); and wherein the emitter structure is "T-shaped" (122), having a lateral portion atop an upright portion, a bottom of the upright portion forms a contact to the base film, and the lateral portion overhangs the base film.

Claims 12-13, 15 and 16-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fujimaki '725 in view of Ko et al. '470. The Examiner states that,

> Fujimaki discloses all of the elements of the claims as set forth above, including forming a nitride stress film atop the base film, but the reference does not explicitly disclose the film to be a means to create compressive strain to increase the mobility of electrons in the device and a means to create tensile strain to increase the mobility of holes in the device, wherein the stress film has at least 0.5 GPa intrinsic stress. Ko et al. teaches a method of forming tensile and compressive stress using a silicon nitride layer (fig. 3g, 238/228) having at least 0.5 GPa stress (¶38) to improve carrier mobility in a transistor (¶43).
>
> It would have been obvious to one of ordinary skill in the art at the time the invention was made to adjust the stress of the nitride layer of Fujimaki as taught by Ko et al. One would have been motivated to do this because Ko et al. taught that creating tensile and compressive stress in a transistor increased the carrier mobility in the device (¶43), thus improving the performance of the device.

Double Patenting

Claims 9-10, 12, 13, 16-18 are rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claim 2 of U.S. Patent No. 7,102,205. Although the conflicting claims are not identical, they are not patentably distinct from each other because claims 9-10, 12, 13, 16-18 of the instant application are anticipated by the limitations of claim 2 of U.S. Patent No. 7,102,205.

A timely filed terminal disclaimer in compliance with 34 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a join research agreement.

The Invention, Generally

The invention is generally directed to creating increased mobility in a bipolar device. The mobility of charge carriers in a bipolar (BJT) device is increased by creating compressive strain in the device to increase mobility of electrons in the device, and creating tensile strain in the device to increase mobility of holes in the device. The compressive and tensile strain are created by applying a stress film adjacent an emitter structure of the device and atop a base film of the device. In this manner, the compressive and tensile strain are located in close proximity to an intrinsic portion of the device. A suitable material for the stress film is nitride. The emitter structure may be "T-shaped", having a lateral portion atop an upright portion, a bottom of the upright portion forms a contact to the base film, and the lateral portion overhangs the base film. (Abstract)

A bipolar device is a semiconductor device, the operation of which is based on the use of both majority and minority carriers (also referred to as "charge carriers"). The majority and minority carriers are either electrons or holes, depending on the polarity of the device. (page 1, paragraph 2)

Lattice strain is known to affect carrier mobility and saturation velocity. Various methods have been shown to cause strain in field effect transistors (FETs). For instance, films which cause tensile strain in the direction of current flow (and sometimes in the direction perpendicular to the direction of current flow) can improve the electron mobility and saturation velocity in FETs. It should be understood that FETs operate fundamentally differently than BJTs. For one thing, there is charge flow in only one direction, which is parallel to the wafer surface. In addition, FETs have a single carrier (electrons for NFET and holes for PFET), and so the application of lattice strain is straightforward to create strain in principally one direction for the single carrier type. (paragraph 10)

Bipolar device (BJT) performance is partly limited by carrier transit time through the space-charge regions and through the neutral base. Low field mobility and saturation velocity

enhancements will benefit this transit time. The performance is also limited by extrinsic resistances in the base, emitter and collector regions. These resistance values are dominated by low field electron and hole mobility and will be affected by strain in the device. Compressive strain will benefit hole mobility, and tensile strain will benefit electron mobility. Applied in the correct locations in the device, strain will significantly improve performance. (paragraph 17)

According to the invention, generally, for an n-p-n BJT hole mobility in the lateral direction is improved by creating lateral compressive strain, and electron mobility in the vertical direction is improved by creating vertical tensile strain. For a p-n-p BJT electron mobility in the lateral direction is improved by creating lateral tensile strain, and hole mobility in the vertical direction is improved by creating vertical compressive strain. (paragraph 21)

The compressive and tensile strain are created by applying a stress film adjacent an emitter structure of the device and atop a base film of the device. In this manner, the compressive and tensile strain are located in close proximity to an intrinsic portion of the device. The strained film is disposed in close proximity to the intrinsic portion of the device. A suitable material for the strained film is nitride. (paragraph 25)

According to the invention, a bipolar device, comprises a collector region, a base film disposed atop the collector region, an emitter structure formed atop the base layer, and a stress film disposed adjacent the emitter structure and atop the base film. The stress film may be a tensile film or a compressive film, depending on the polarity of the bipolar device. (paragraph 26)

The emitter structure may be "T-shaped", having a lateral portion atop an upright portion, a bottom of the upright portion forms a contact to the base film, and the lateral portion overhangs the base film. (paragraph 27)

FIG. 3 is a simplified cross-sectional view of a BJT 300, fabricated according to the techniques of the present invention. (paragraph 33)

The BJT 300 comprises a collector region 302, a base film 304 disposed atop the collector region 302 and an emitter structure 306 formed atop the base layer 304. Generally, strain in the device is created by removing the insulator layer 208 (see FIG. 2) and replacing it with (applying) a film 308 which creates strain(s) in the intrinsic region of the device. The "stress" film 308 preferably provides both compressive and tensile strain in this region. In this example, the film 308 is adjacent the upright portion of the emitter structure 306, and atop the base film 304. The film 308 is disposed in this region because it is in close proximity to the intrinsic portion of the device. (The intrinsic region of the device is the portion directly under the vertical portion of the emitter polysilicon, such that it encompasses the flow of carriers from the neutral emitter into the neutral collector. The portions that provide connectivity, i.e. the emitter polysilicon, the portion of the base layer not under the emitter polysilicon, and most of the collector layer are considered extrinsic.) (paragraph 42)

For a n-type (n-p-n) BJT, the film 308 is a compressive film. Because of the T-shaped structure of the emitter and the location of the film 308 - namely, adjacent the emitter structure and atop the base film, the film 308 imposes tensile strain in the vertical (as viewed) direction and compressive strain in the horizontal direction. (For a p-type (p-n-p) device, the film would be a tensile film, resulting in compressive strain in the vertical direction and tensile strain in the horizontal direction.) (paragraph 43

By removing the previous oxide film (208, FIG. 2) and replacing it with an intentionally stress film, the strain may be placed (located) in close proximity to the intrinsic portion of the device. The resultant increase in carrier mobility and saturation velocity has the effect of providing higher current drive and shorter transit time for improved RF device performance. (paragraph 44)

Generally, the oxide 208 is removed late in the process, and the film 308 is deposited as late in the process as possible so that strains will be preserved. A stress nitride film with at least 0.5GPa (Giga-Pascal) intrinsic stress is suitable for use as the film 308. (paragraph 45)

FIGs. 4, 4A-4F are cross-sectional views of a sequence of steps used to fabricate a BJT, according to the invention. (paragraph 33) (notice the similarity between FIG. 4F and FIG. 3.)

FIG. 5 is a cross-sectional view of a complete BJT, formed according to the steps illustrated in FIGs. 4, 4A-4F, according to the invention. (paragraph 34)

The References, Generally

Fujimaki (6,780,725) discloses a method for forming a semiconductor device including forming vertical npn and pnp transistors by exposing the epitaxial layer, forming a monocrystal layer and adjusting the impurity concentration in the epitaxial layer. A method of manufacturing vertical NPN and PNP transistors on a substrate includes forming a first oxide film, a P-polycrystal silicon film, and a second oxide film successively on N-silicon epitaxial film on the substrate. An opening is made in the first oxide film to expose the N-silicon epitaxial film and a bottom of the P-polycrystal silicon film anisotropically etching the second oxide film and the P-polycrystal silicon film, and then isotropically etching the exposed first oxide film. A part of the opening is plugged by growing a selective epitaxial layer including a P-monocrystal layer from the surface of the N-silicon epitaxial film, and growing a polycrystal layer from the bottom of the P-polycrystal silicon film. Then, within a PNP transistor section, position and impurity concentration of a P-N junction are adjusted by self-aligned implanting or diffusing of P-impurities into the N-silicon epitaxial layer through the opening.

Ko (2005/0035470) discloses strained channel complementary field-effect transistors and methods of manufacture. A transistor includes a gate dielectric overlying a channel region. A source region and a drain region are located on opposing sides of the channel region. The channel region is formed from a first semiconductor material and the source and drain regions are formed from a second semiconductor material. A gate electrode overlies the gate dielectric. A pair of spacers is formed on sidewalls of the gate electrode. Each of the spacers includes a void adjacent the channel region. A high-stress film can overlie the gate electrode and spacers.

Commonly-owned 7,102,205 (Chidambarrao) discloses bipolar transistor with extrinsic stress

layer. A method of increasing mobility of charge carriers in a bipolar device comprises the steps of: creating compressive strain in the device to increase mobility of holes in an intrinsic base of the device; and creating tensile strain in the device to increase mobility of electrons in the intrinsic base of the device. The compressive and tensile strains are created by forming a stress layer in close proximity to the intrinsic base of the device. The stress layer is at least partially embedded in a base layer of the device, adjacent an emitter structure of the device. The stress layer has different lattice constant than the intrinsic base. Method and apparatus are described.

Traversing the Rejection(s)

Fujimaki (6,780,725) discloses vertical NPN and PNP transistors.

Fujimaki FIGS. 1A to 1D are diagrams showing a structure of a first semiconductor device, and do not seem to be relevant.

4 - active collector region

5 - epitaxial layer serving as base of the transistor

16 – a T-shaped structure (Fig 1D) is a polysilicon connection

Fig. 2 –left shows PNP. Fig. 2 – right shows NPN. As discussed in Fujimaki,

> After that, an N+ -BL layer 105, to serve as a buried diffusion zone of the NPN transistor, is formed by a second exposure/diffusion process, and then an N-epitaxial layer 106 ... is formed ... Next, a field oxide film 107 is formed by a process including a LOCOS process and a third exposure process, and then the monocrystal silicon of the active region is exposed (S105a, S105b). (col 7, lines 4-11)
>
> An N-silicon film is grown epitaxially to a thickness of about 50 nm in such an atmosphere, and subsequently, an N-epitaxial film 118a .... is grown. (col 8, lines 22-25)
>
> ... a silicon nitride film 117 is formed to a thickness of 150 nm to cover the entire substrate surface, and then it is subjected to anisotropic etch. As a result, the silicon nitride film remains on the sidewall of the opening (S111a, S111b). (col 8, lines 6-10)

Regarding "stress", Fujimaki discloses,

> Next, the exposed thermally-oxidized film (equivalent to 507 in FIG. 9) is removed with the PNP transistor section and the NPN transistor section being protected by a resist pattern formed by an eleventh exposure process. Then after completion of a side etch to a depth of about 250 nm and a removal of the resist pattern, selective epitaxial growth is carried out. The grown epitaxial film has a double-layer structure. A first layer is a 100 nm-thick SiGe epitaxial layer containing 40% Ge (an N--SiGe layer 606 or a P--SiGe layer 612). A second layer is a 25 nm-thick silicon epitaxial layer containing no Ge (a polycrystal silicon layer 607 or 613). During the epitaxial growth of the first layer, **stress relaxation** occurs at an interface between the crystal face of the substrate and the SiGe epitaxial layer. However, since the second layer is as thin as 25 nm, **stress relaxation** does not occur at an interface during the epitaxial growth of the second layer although the first layer contains a high concentration of Ge. (column 14, last paragraph: emphasis supplied)
>
> Accordingly, the epitaxial SiGe layer has an equant crystal structure, whereas the epitaxial silicon layer has a dimetric crystal structure undergoing **stress**. Since ions are implanted to the transistor sections to increase impurity concentrations of their surfaces before carrying out the epitaxial growth, the entire epitaxial film becomes N type for the PMOS transistor section, whereas it becomes P type for the NMOS transistor section due to the auto-doping effect. The structures obtained by the above processes are shown in a magnified form at steps S601a, S601b. (column 15, first paragraph: emphasis supplied)
>
> Although the MOS transistor is restricted to the ring-shaped structure as in the case of the second semiconductor device previously explained, it can be formed within a sufficiently small area by micromachining technology, and its operation speed is high enough since the channel is on the silicon film undergoing stress at the relaxed SiGe layer and accordingly the carrier mobility is high. (column 16, lines 17-23)

As noted above, Fujimaki uses SiGe (612) and Si (607, 613), epitaxially grown, for stress, in

PMOS and NMOS transistors (see FIG. 11). See also FIG. 12 for NPN and PNP transistors.

Fujimaki discloses a silicon nitride layer 110, for both PNP and NPN (see FIGs. 2,3).

Subsequently, this polycrystal silicon layer 109 is patterned by a fourth exposure process, and then, a silicon nitride film 110 is formed to a thickness of 200 nm (S106a, S106b)

Subsequently, the remaining silicon nitride film 110 is removed completely by use of hot phosphoric acid, and then, another silicon nitride film 113 is formed to a thickness of 200 nm (S109a, S109b).

After that, the oxide film mask and the silicon nitride film 113 are removed, and then another silicon nitride film 114 is formed to cover the entire substrate surface (S109a, S109b).

In all instances, the silicon nitride film 110/113/114 appears to be separated from what appears to be the base layer (N-Epi 106) by a thermally-oxidized film 108, followed by a highly boron-doped polycrystal silicon layer 109

In the present invention, the stress film comprises nitride. The present invention is directed to a compressive stress nitride film applied atop a silicon layer to create and maintain a compressive and tensile strain in the silicon layer. The creation and maintenance of the compressive and tensile strain enhances the lateral hole mobility and the vertical electron mobility. The stress layer is put on last, to preserve the stress in the silicon layer.

As best seen in Fig. 4F the nitride film 450 is applied directly across the silicon layer 420. The nitride film extends a significant distance across layer 420.

Also, from FIG. 3 of the present invention it can be seen that the compressive nitride stress film covers the vertical and horizontal surfaces of the T-shaped emitter 306. See also 450, FIG 4F. Note, for example,

Next, as shown in FIG. 4F, a conformal stress film 450 (compare 308) is deposited, covering all exposed surfaces. This film is deposited typically with either a PECVD or an RTCVD process. In the case of the PECVD process, the stress is imposed through

modifying the RF power of the deposition conditions and in the case of RTCVD the stress is imposed through modifying the precursor.

Claim 9 is amended to clarify the differences between the present invention, and Fujimaki, regarding nitride and covering all of the exposed surfaces of the emitter.

Additionally, in Fujimaki, the nitride film (Si_3N_4), as best seen in Fig. 12, is only disposed on the side edges of cap silicon layer 621. Fujimaki's silicon layer 621 is comparable to the silicon layer 420 of the present invention. In the present invention, the stress layer is put on last, to preserve the stress in the silicon layer. Fujimaki does further steps, after the nitride film has been applied, which reduces stress in the nitride layer.

In light of the above, it is believed that an extensive discussion of the Ko et al. reference is not required. Ko doesn't overcome the missing limitation, i.e., a compressive stress nitride film applied atop a silicon layer to create and maintain a compressive and tensile strain in the silicon layer. See claims, as amended herewith.

Double Patenting

Claim 2 of Chidambarrao reads, as follows:

2. Bipolar device comprising:

a collector region,

a base layer disposed atop the collector region;

an emitter structure formed atop the base layer;

an extrinsic stress layer disposed adjacent the emitter structure and at least partially embedded in the base layer;

the extrinsic stress layer is disposed over an intrinsic base formed in the base layer of the device; and

for an npn bipolar device, the extrinsic stress layer creates vertical tensile strain in the intrinsic base, below the emitter structure, increasing electron mobility in the intrinsic base and creates horizontal compressive strain in the intrinsic base, increasing hole mobility in

the intrinsic base, below the emitter structure; and

for a pnp bipolar device, the extrinsic stress layer creates vertical compressive strain in the intrinsic base region below the emitter structure, increasing hole mobility in the intrinsic base and creates horizontal tensile strain in the intrinsic base region below the emitter structure, increasing electron mobility in the intrinsic base.

There are similarities, and differences, between Chidambarrao (7102205) and the Patent application. Note that the inventors are the same in both cases. In light of the significant differences between the two, two separate patent applications were filed. Chidambarrao has issued as a patent. Their general purpose is similar in the sense that it is desired to stress the base. The "flows" seemingly look similar, but by looking at the structures below it can be seen that there are significant differences in the process, sequence, and final structure.

In Chidambarrao FIGs 2B, 2C, 3 it can be seen that first the base film is thinned, then a strain film is deposited. The strain film is embedded. "The stress layer is at least partially embedded in a base layer of the device, adjacent an emitter structure of the device." (Abstract)

As further noted in the specification of Chidambarrao,

FIGS. 2B and 2C illustrate an embodiment of a BJT 220, according to the invention. A collector region 202 is defined in the substrate between two STI region, a base film 204 is disposed atop the collector region, an emitter structure 206 is disposed atop the base film, and spacers are formed on the sides of the emitter structure. Typical dimensions for these elements can be as in the BJT 200.

Recesses are formed in the base film, on both sides of the emitter structure (i.e., adjacent the sidewall spacers) using any suitable etching process. The recesses are suitably approximately 10 to 25 nm in depth (vertical, in the figure), and extend laterally beyond the collector region and over the STI. The thus "thinned" layer of the base film has a thickness of approximately 25 to 45 nm.

The recesses are then filled with epitaxially grown stress layer using known processes. This includes overfilling the recesses. The stress layer thus formed may have a thickness of approximately 10 100 nm (essentially equal to the depth of the recesses). This stress layer may be doped to link with the intrinsic base under the emitter structure.

The final structure, shown in FIG. 2C includes emitter polysilicon and may include a raised doped extrinsic base for lower resistance.

FIG. 3 illustrates the strain in the final structure of FIG. 2C. The SiGe layer ("stress layer") creates a tensile strain in the vertical direction, parallel to the direction of electron flow as shown by the vertical double-headed arrow in FIG. 2D. (The electron flow is shown by the vertical single-headed arrow in FIG. 1). The tensile strain will enhance electron mobility and reduce transit time and increase current and transconductance. The stress layer also creates a compressive strain perpendicular to the direction of electron flow as shown by the horizontal single-headed arrow in FIG. 3. (There would be another inward-pointing arrow under the left side of the emitter, if it were shown in the view of FIG. 3). This compressive strain enhances hole mobility in the intrinsic base region.

Claim 2 of Chidambarrao recites,

an extrinsic stress layer disposed adjacent the emitter structure and at least partially embedded in the base layer;

Claim 1 of Chidambarrao recites,

an extrinsic stress layer disposed adjacent the emitter structure and at least partially embedded in the base layer;

Please take note of the emphasis on "embedded", the meaning of which is believed to be non-ambiguous. An example of prior art "embedded" (for CMOS) is set forth in the specification,

"A 90 nm High Volume Manufacturing Logic Technology Featuring Novel 45 nm Gate Length Strained Silicon CMOS Transistors", T. Ghani et al., Portland Technology

Development, Intel Corp., Hillsboro, Oreg., 0-7803-7873 Mar. 3, 2003, IEEE describes the details of a strained transistor architecture which is incorporated into a 90 nm logic technology on 300 mm wafers. The strained PMOS transistor structure features an epitaxially grown strained SiGe film **embedded** in the source drain regions. Dramatic performance enhancement relative to unstrained devices are reported. Ghani FIG. 1 shows a PMOS transistor with a strained epitaxial SiGe film embedded into the source drain region to induce compressive strain in the channel region.

Also, in the more specific example given in the Chidambarrao specification,

Generally, the stress layer is at least partially embedded in the underlying base layer. The intrinsic base (see FIG. 4B, 421) is typically silicon (Si) or silicon germanium (SiGe).

.. and ..

The stress layer is at least partially embedded in a base layer of the device, adjacent an emitter structure of the device.

... and ...

Since the stress layer may be only partially embedded, as described below, it can have the same or even greater thickness than the underlying base film.

... and ...

Generally, the stress layer is at least partially embedded in the underlying base layer, and has a different lattice constant than the underlying base layer, thereby causing stress in the regions next to and below it.

... as well as ...

Next, as shown in FIG. 4E, a stress layer 450 is epitaxially grown. The stress layer is shown as 450 over the silicon 420 and as 451 over the SiGe 421'. The stress layer is grown back up to at least the height of the oxide 422, including beyond the original height of the thinned layer 421', in either case it is embedded.

The stress film (308) of the present invention is not embedded. As noted in the specification,

" ... the film 308 is adjacent the upright portion of the emitter structure 306, and atop the base film 304."

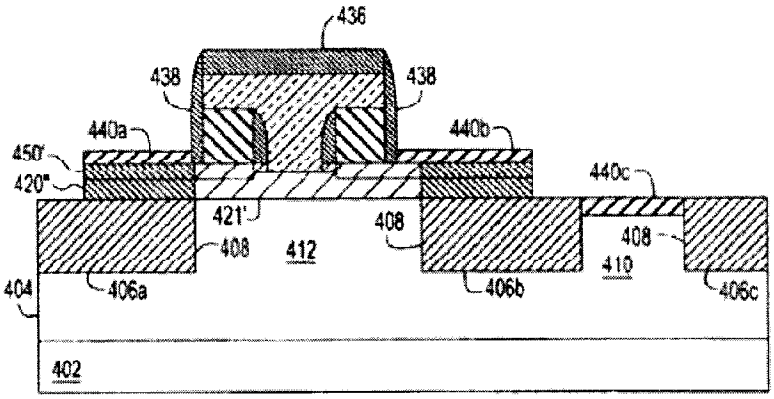
Additional comments relating to Chidambarrao

The Chidambarro patent (7102205) uses eSiGe, which requires a recess and SiGe growth and is therefore embedded. Further the claims indicate epitaxy with crystallinity and lattice constant driven strain.

In the present patent application, there is no recess, the process is simpler, and uses stressed nitride as a basis for stress transfer.

Compare, for example, FIG. 4J (front page) of Chidambarrao with FIG. 5 of the patent application.

Chidambarrao, FIG. 4J



Patent Application, FIG. 5

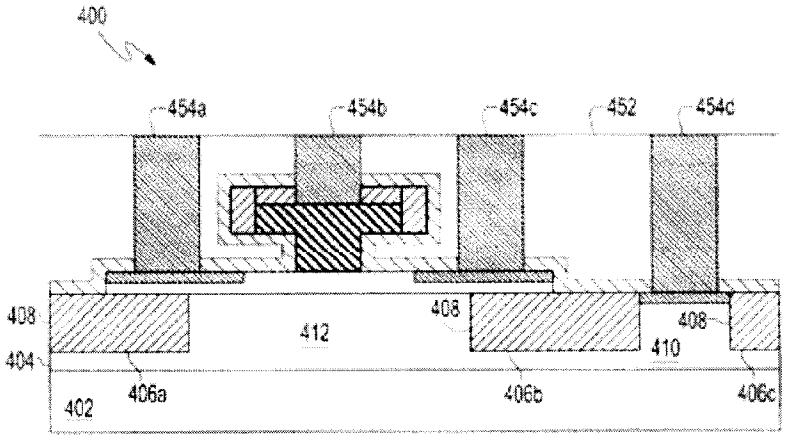


FIG. 5

In Chidambarrao , the stressor 450 is SiGe grown epitaxially on 420.

In the Patent Application, the stressor 450 is nitride, and is not grown epitaxially, rather it is deposited, and therefore completely wraps around the T-shaped emitter (430, also 306). It also comes later in the process.

The stress contours and stress values are very different as can be seen in the stress contour and cutline figures. (Chidambarrao FIGs. 6,7,8; Patent Application FIGs. 6,7,8) In Chidambarrao the stress edges are further away while in the Patent Application the stressor is closer.

Since Chidambarrao uses epitaxy, the gap fill under the T part of the emitter needs to be an oxide 428 and emitter spacers 434 are also needed. In the Patent Application these are absent and the stressor material (nitride) replaces these material systems in the final structure.

Chidambarrao discloses a "larger lattice" mismatch stress using material "SiGe" or "SiC" that is "partially embedded" (see, for example, claim 1). In contrast thereto, the Patent Application discloses "intrinsic stress" that is "atop a base film of the device" with "close proximity" and

being "silicon nitride". These two features are very different than one another.

In the present invention, the stress film is not embedded. Also, **Claim 9** is amended to clarify the differences between the present invention and Chidambarrao.

The double patenting objection should be withdrawn.

Amendments to the Claims

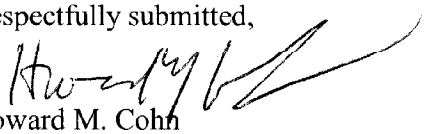
Claim 9 is amended to include limitations from claim 11 ("T-shaped" emitter), claim 14 (nitride), plus " the stress film covers exposed surfaces of the emitter structure" (as discussed hereinabove) and should now be deemed allowable.

Claims 10, 12, 13, 15, 16 and 17 depend upon claim 9 and should also be deemed allowable.

Conclusion

Applicant respectfully requests that a timely Notice of Allowance be issued in this case.

Respectfully submitted,



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